In the Claims:

Please amend claim 6. The claims are as follows:

1. (Previously presented) An oscillator delay stage circuit operating between first and second operating voltages, wherein the first operating voltage is higher than the second operating voltage, the oscillator delay stage circuit comprising:

(a) an inverting circuit including an input node and an output node,

wherein the inverting circuit is configured to receive an input signal from the input node and generate an output signal to the output node, and

wherein the inverting circuit is further configured to increase the output signal in voltage in response to the input signal decreasing in voltage and to decrease the output signal in voltage in response to the input signal increasing in voltage; and

(b) a control circuit including (i) a first switch circuit and a first resistance adjusting circuit electrically coupled in series between the output node and the second operating voltage, and (ii) a second switch circuit and a second resistance adjusting circuit electrically coupled in series between the output node and the first operating voltage,

wherein in response to the input signal increasing in voltage towards the first operating voltage, the first switch circuit is configured to decrease in resistance,

wherein in response to the input signal decreasing in voltage towards the second operating voltage, the second switch circuit is configured to decrease in resistance,

wherein the first resistance adjusting circuit is configured to receive as input an external control signal and to change in resistance in response to a change of the external control signal,

wherein the second resistance adjusting circuit is configured to receive as input the external control signal and to change in resistance in response to a change of the external control signal, and

wherein the second resistance adjusting circuit comprises a first n-channel transistor.

2. (Previously presented) The oscillator delay stage circuit of claim 1, wherein the first switch circuit comprises a second transistor having a gate terminal configured to receive the input signal,

wherein the first resistance adjusting circuit electrically couples the first switch circuit to the output node, and

wherein the second resistance adjusting circuit electrically couples the second switch circuit to the output node.

3. (Previously presented) The oscillator delay stage circuit of claim 2, wherein the second transistor is an n-channel transistor.

4. (Previously presented) The oscillator delay stage circuit of claim 1, wherein the first resistance adjusting circuit comprises a third transistor having a gate terminal configured to receive the external control signal.

5. (Previously presented) The oscillator delay stage circuit of claim 4, wherein the third transistor is an n-channel transistor.

6. (Currently amended) ~~An oscillator delay stage circuit operating between first and second operating voltages, wherein the first operating voltage is higher than the second operating voltage,~~ the ~~oscillator delay stage circuit comprising:~~

~~(a) an~~ inverting ~~circuit including an input node and an output node;~~

wherein the inverting circuit is configured to receive an input signal from the input node and generate an output signal to the output node, and

wherein the inverting circuit is further configured to increase the output signal in voltage in response to the input signal decreasing in voltage and to decrease the output signal in voltage in response to the input signal increasing in voltage; and

(b) a control circuit including a first switch circuit and a first resistance adjusting circuit electrically coupled in series between the output node and the second operating voltage,

wherein in response to the input signal increasing in voltage towards the first operating voltage, the first switch circuit is configured to decrease in resistance, and

wherein the first resistance adjusting circuit is configured to receive as input an external control signal and to change in resistance in response to a change of the external control signal, The oscillator delay stage circuit of claim 1, wherein the inverting circuit comprises a CMOS inverter.

7. (Original) The oscillator delay stage circuit of claim 1, wherein the control circuit further comprises an extrinsic capacitor electrically coupled between the output node and the second operating voltage.

8. (canceled)

9. (Previously presented) An oscillator delay stage circuit operating between first and second operating voltages, wherein the first operating voltage is higher than the second operating voltage, the oscillator delay stage circuit comprising:

(a) an inverting circuit including an input node and an output node,

wherein the inverting circuit is configured to receive an input signal from the input node and generate an output signal to the output node, and

wherein the inverting circuit is further configured to increase the output signal in voltage in response to the input signal decreasing in voltage and to decrease the output signal in voltage in response to the input signal increasing in voltage; and

(b) a control circuit including a first switch circuit and a first resistance adjusting circuit electrically coupled in series between the output node and the first operating voltage,

wherein in response to the input signal decreasing in voltage towards the second operating voltage, the first switch circuit is configured to decrease in resistance,

wherein the first resistance adjusting circuit is configured to receive as input an external control signal and to change in resistance in response to a change of the external control signal,

wherein the first resistance adjusting circuit comprises a first n-channel transistor, and

wherein the first resistance adjusting circuit electrically couples the first switch circuit to the output node.

10. (Previously presented) The oscillator delay stage circuit of claim 9, wherein the first switch circuit comprises a second transistor having a gate terminal configured to receive the input signal.

11. (Previously presented) The oscillator delay stage circuit of claim 10, wherein the second transistor is a p-channel transistor.

12. (Previously presented) The oscillator delay stage circuit of claim 9, wherein the first n-channel transistor comprises a gate terminal configured to receive the external control signal.

13. (canceled)

14. (Original) The oscillator delay stage circuit of claim 9, wherein the inverting circuit comprises a CMOS inverter.

15. (Original) The oscillator delay stage circuit of claim 9, wherein the control circuit further comprises an extrinsic capacitor electrically coupled between the output node and the first operating voltage.

16. (canceled)

17. (Previously presented) A method for signal generation, the method comprising the steps of:
(a) providing a voltage-controlled oscillator comprising N oscillator delay stage circuits operating between first and second operating voltages, N being an odd integer, the first operating voltage being higher than the second operating voltage, wherein each of the N oscillator delay stage circuits comprises:

(i) an inverting circuit including an input node and an output node, and

(ii) a control circuit including a switch circuit and a resistance adjusting circuit electrically coupled in series between the output node and the first operating voltage,

wherein the resistance adjusting circuit comprises a first n-channel transistor;
(b) applying to the resistance adjusting circuit an external control signal so as to achieve a target operating frequency for the voltage-controlled oscillator;

(c) in response to an input signal decreasing in voltage at the input node,

(i) using the inverting circuit to increase an output signal in voltage at the output node, and

(ii) decreasing the resistance of the switch circuit.

18. (Previously presented) The method of claim 17, wherein the switch circuit comprises a second transistor having a gate terminal configured to receive the input signal, wherein the resistance adjusting circuit electrically couples the switch circuit to the output node.

19. (Previously presented) The method of claim 17, wherein the first n-channel transistor comprises a gate terminal configured to receive the external control signal.

20. (Original) The method of claim 17, wherein the inverting circuit comprises a CMOS inverter.